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Pandey et al.

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(54) **METHODS OF FORMING TRANSISTORS**

(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)

(72) Inventors: **Deepak Pandey**, Boise, ID (US); **Haitao Liu**, Boise, ID (US); **Fawad Ahmed**, Boise, ID (US); **Kamal M. Karda**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

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(51) **Int. Cl.**

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H01L 29/06	(2006.01)
H01L 29/66	(2006.01)
H01L 21/306	(2006.01)
H01L 21/308	(2006.01)
H01L 29/10	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/0692*** (2013.01); ***H01L 21/308*** (2013.01); ***H01L 21/30604*** (2013.01); ***H01L 29/0649*** (2013.01); ***H01L 29/1083*** (2013.01); ***H01L 29/66795*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/30604; H01L 21/308; H01L 29/1083

See application file for complete search history.

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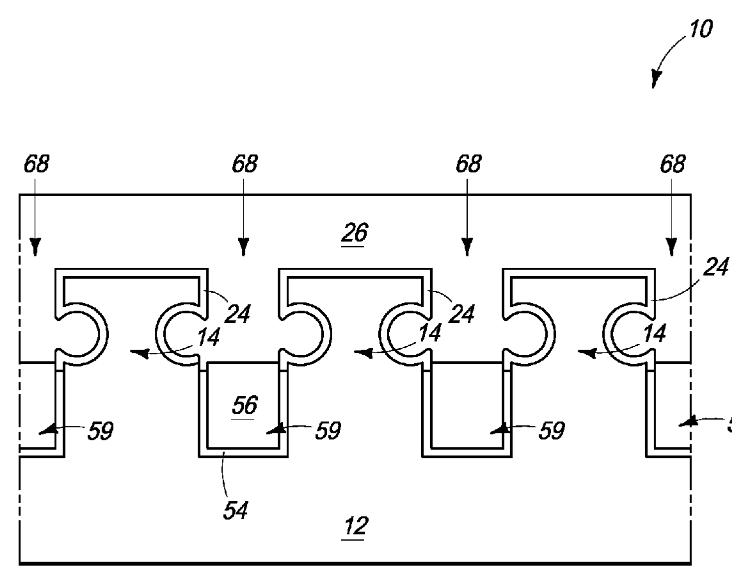
Primary Examiner — Richard Booth

(74) *Attorney, Agent, or Firm* — Wells St. John P.S.

(57) **ABSTRACT**

Some embodiments include methods of forming transistors. Recesses are formed to extend into semiconductor material. The recesses have upper regions lined with liner material and have segments of semiconductor material exposed along lower regions. Semiconductor material is isotropically etched through the exposed segments which transforms the recesses into openings having wide lower regions beneath narrow upper regions. Gate dielectric material is formed along sidewalls of the openings. Gate material is formed within the openings and over regions of the semiconductor material between the openings. Insulative material is formed down the center of each opening and entirely through the gate material. A segment of gate material extends from one of the openings to the other, and wraps around a pillar of the semiconductor material between the openings. The segment is a gate of a transistor. Source/drain regions are formed on opposing sides of the gate.

32 Claims, 14 Drawing Sheets



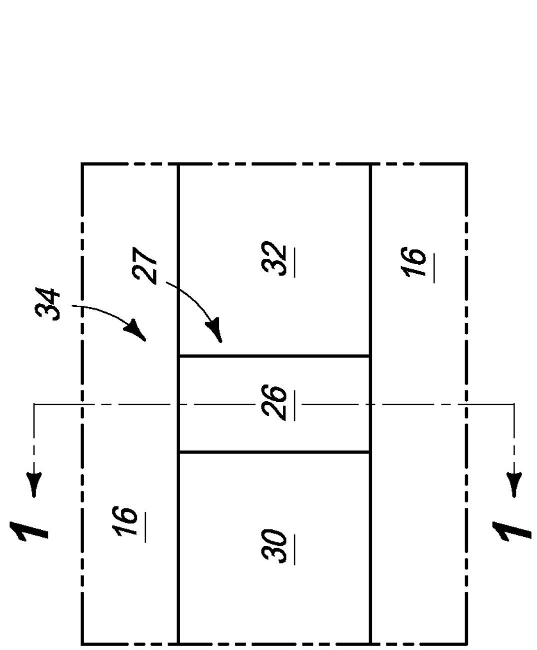


FIG. 1A

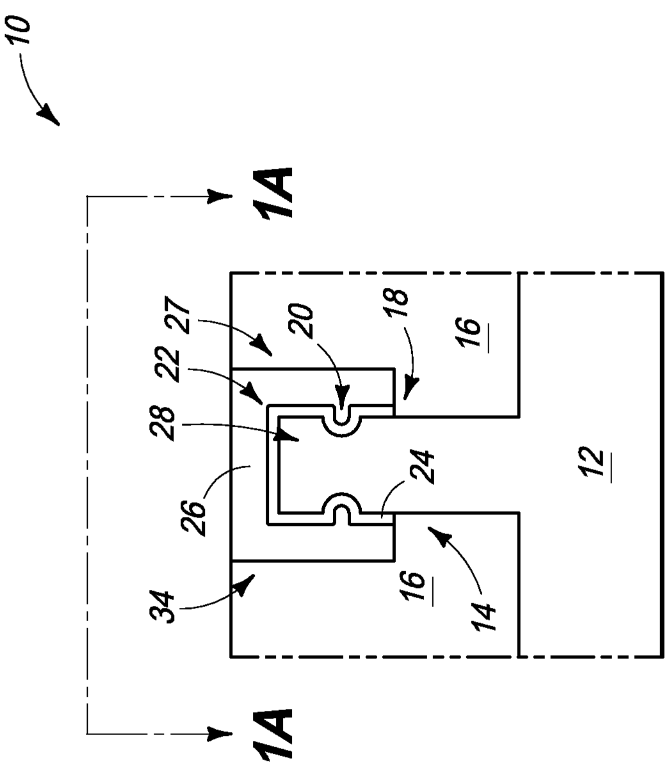


FIG. 1

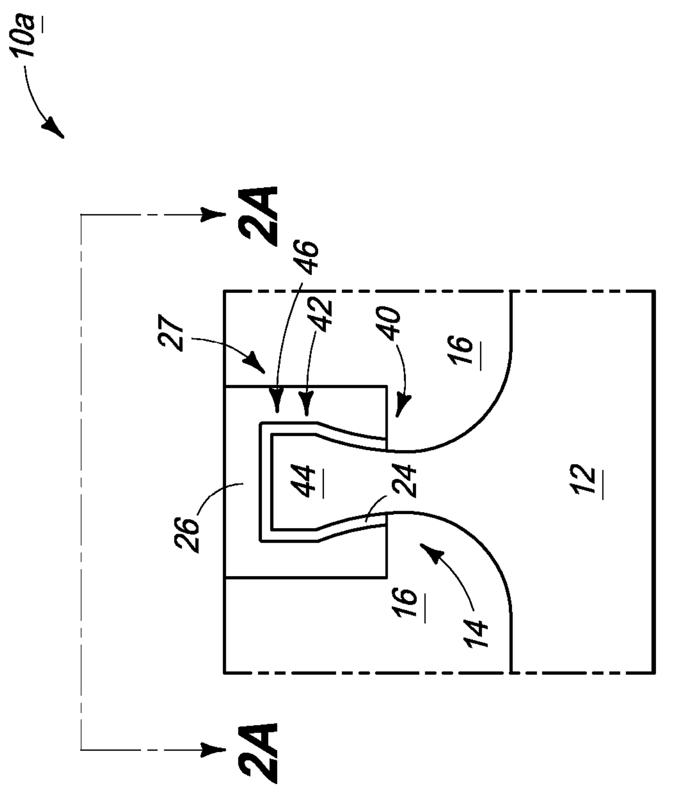


FIG. 2

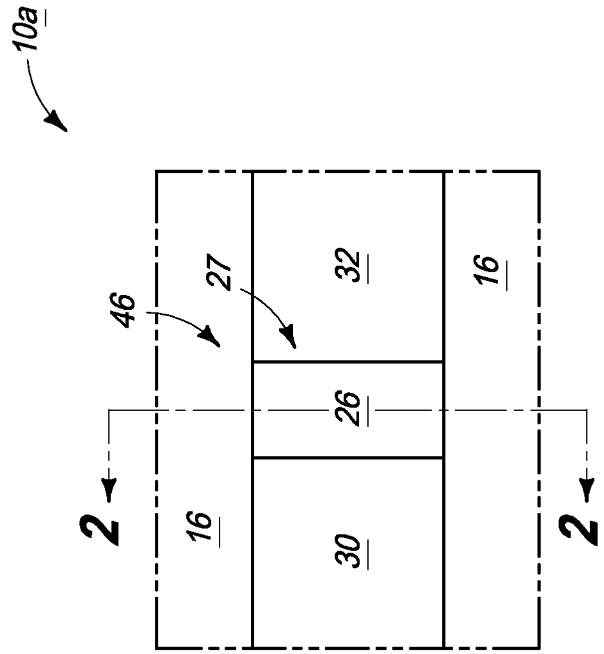


FIG. 2A

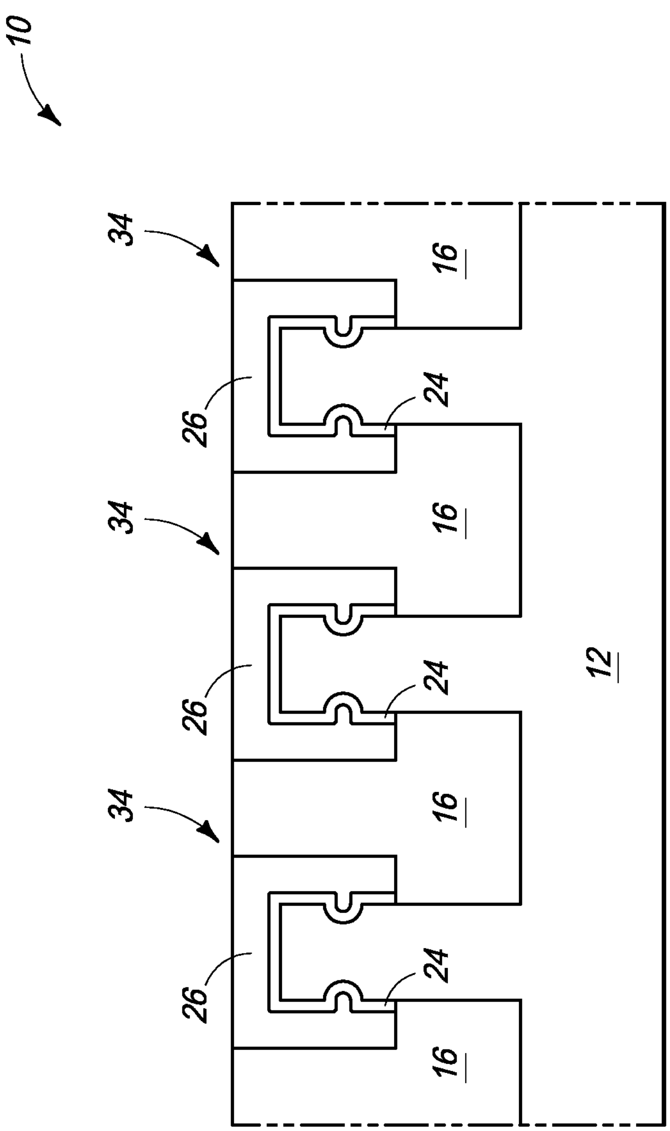


FIG. 3

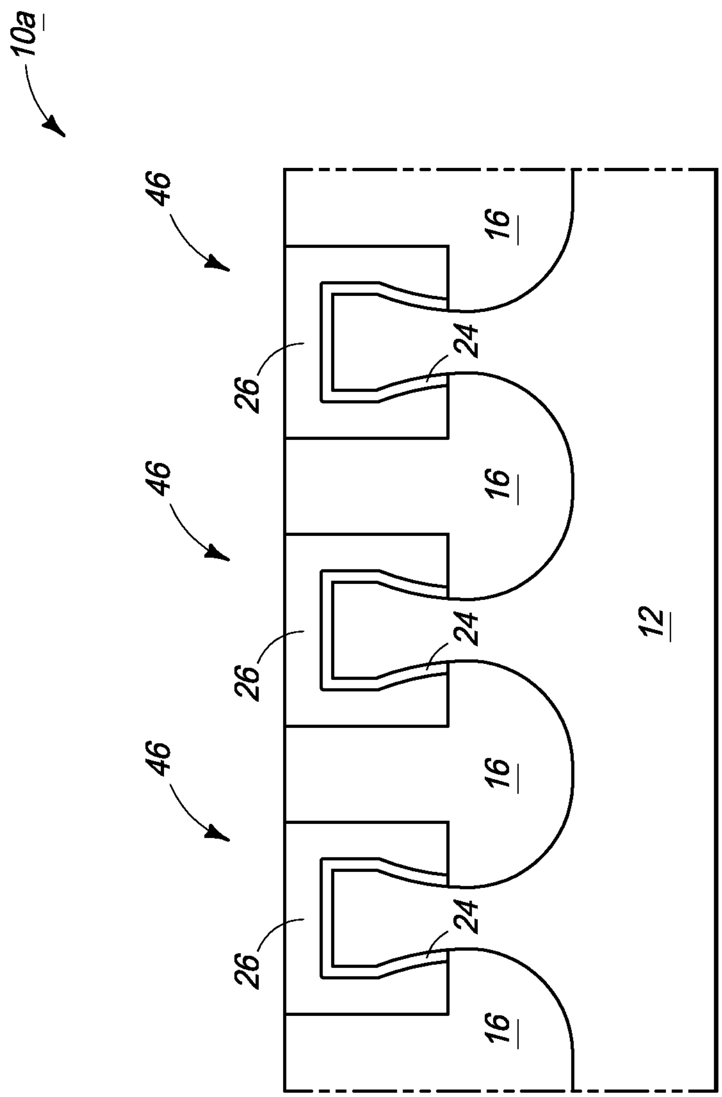
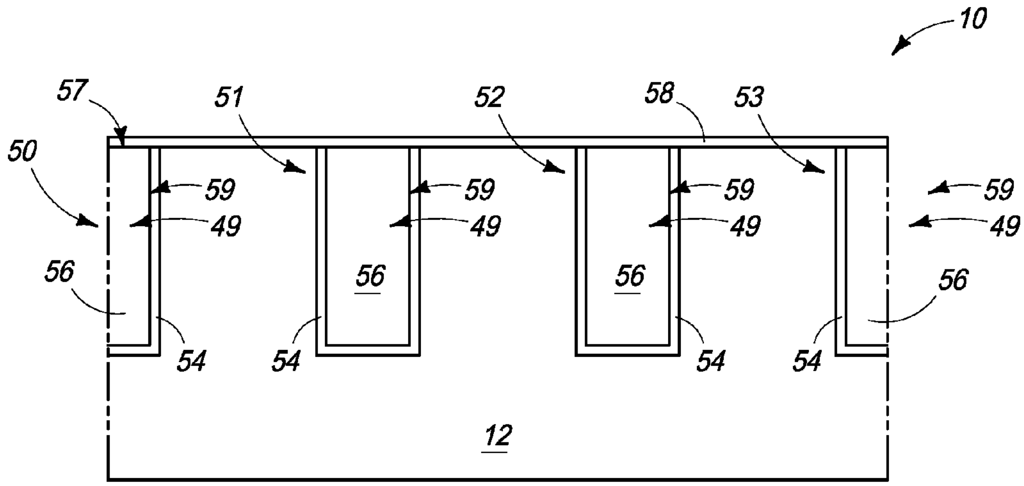


FIG. 4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51
52
58
53
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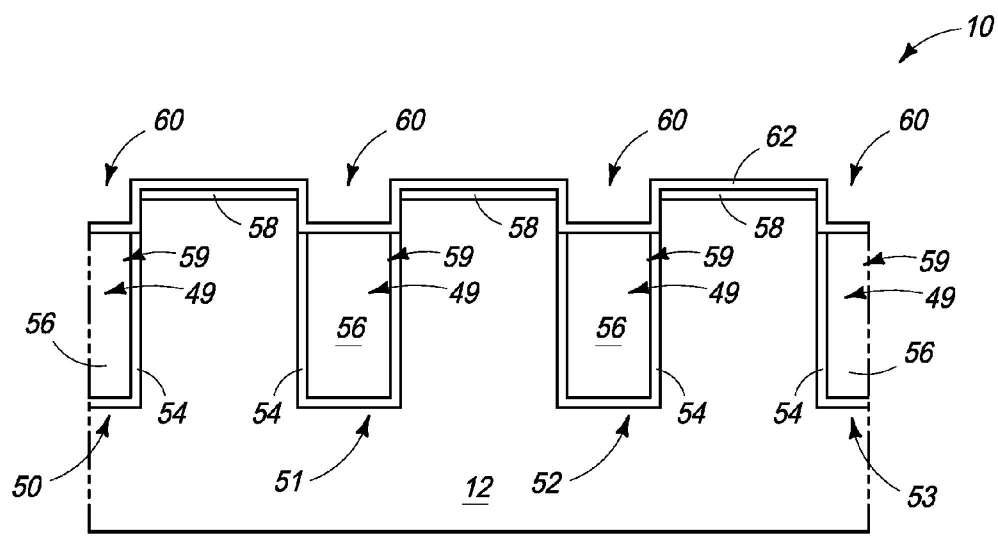
54
12

FIG. 5


10
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62
58
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59
49
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54
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54
50
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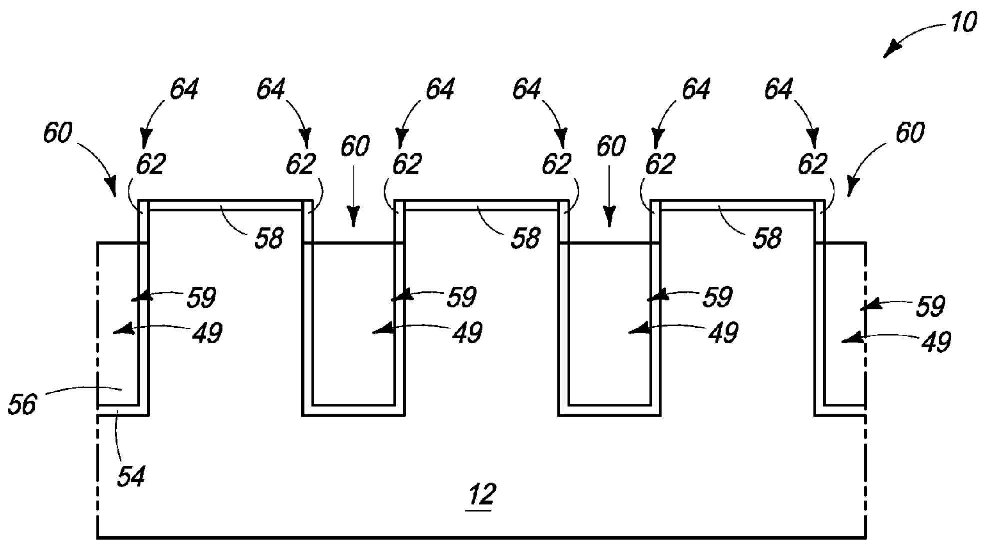
53
12

FIG. 6


10
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62
60
62
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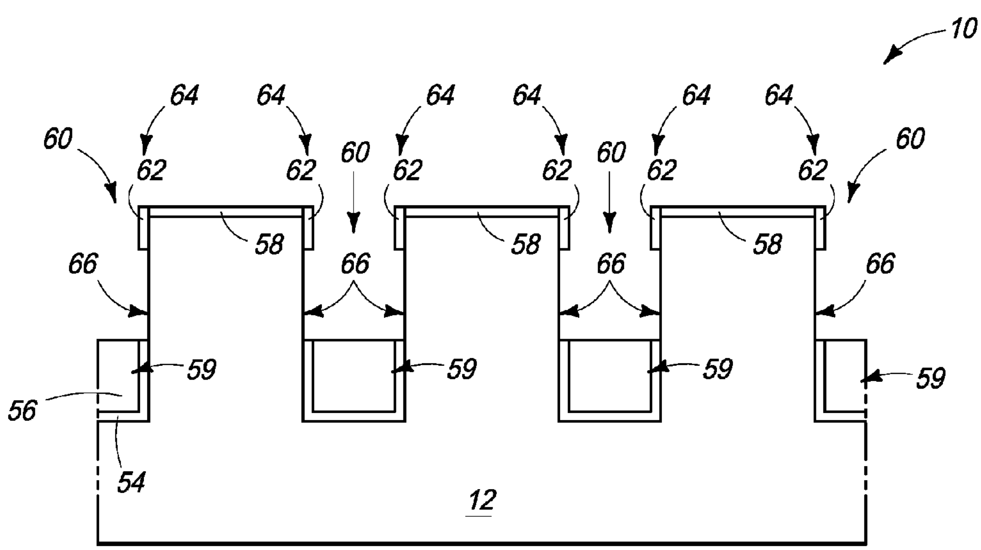
56
54
12

FIG. 7


10
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62
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60
62
62
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62
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58
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58
66
66
66
66
59
59
59
59
56
54
12

FIG. 8

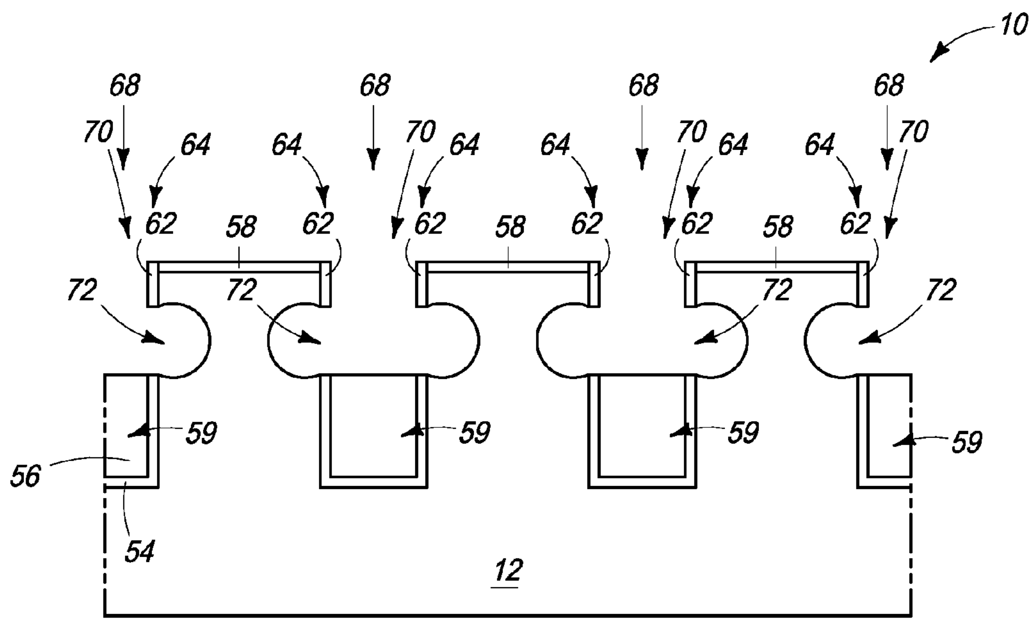


FIG. 9

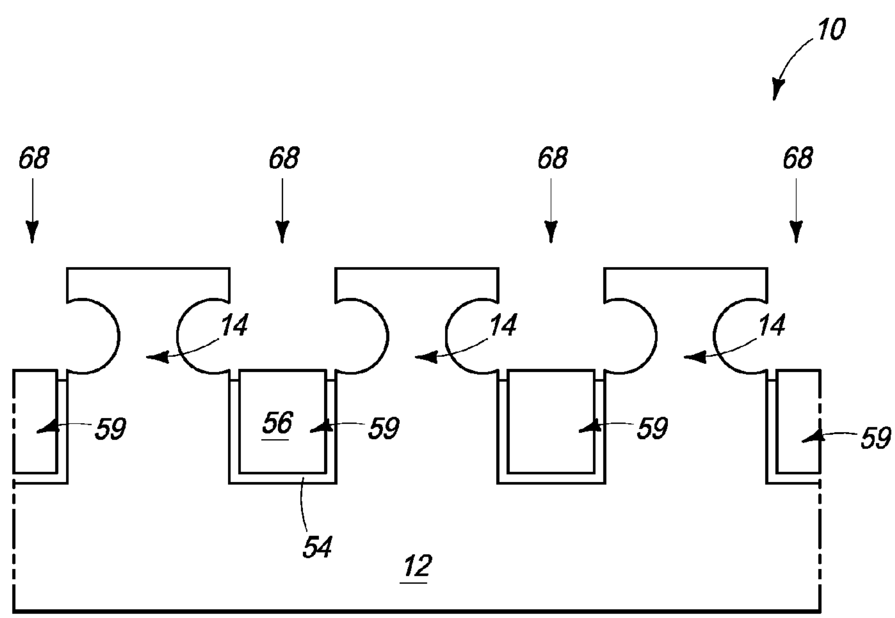


FIG. 10

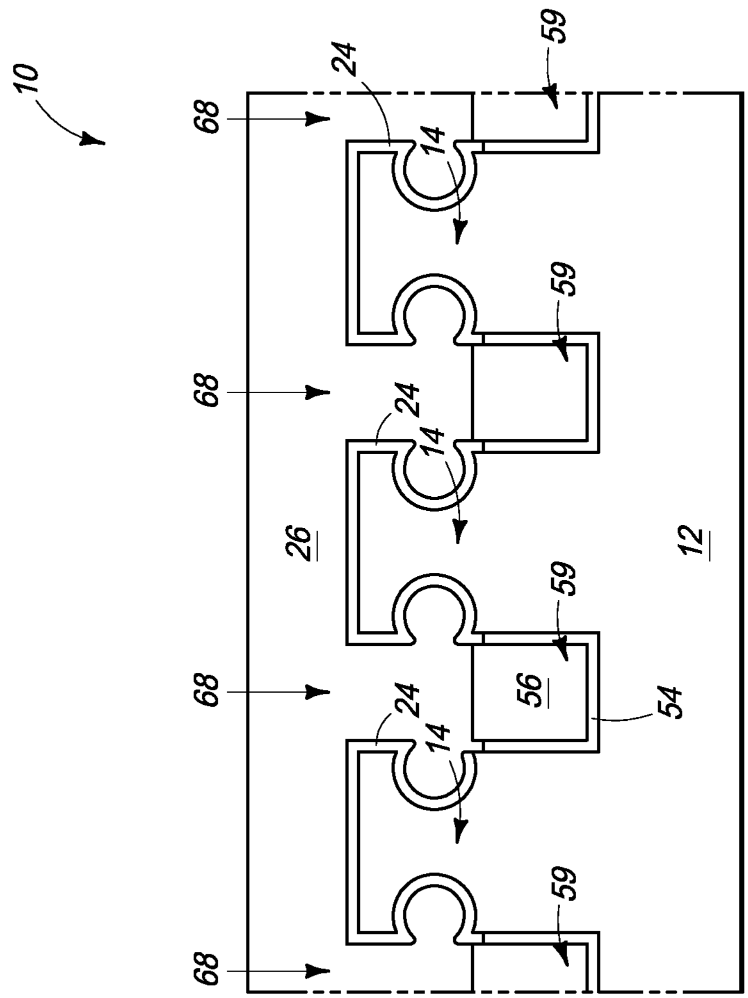


FIG. 11

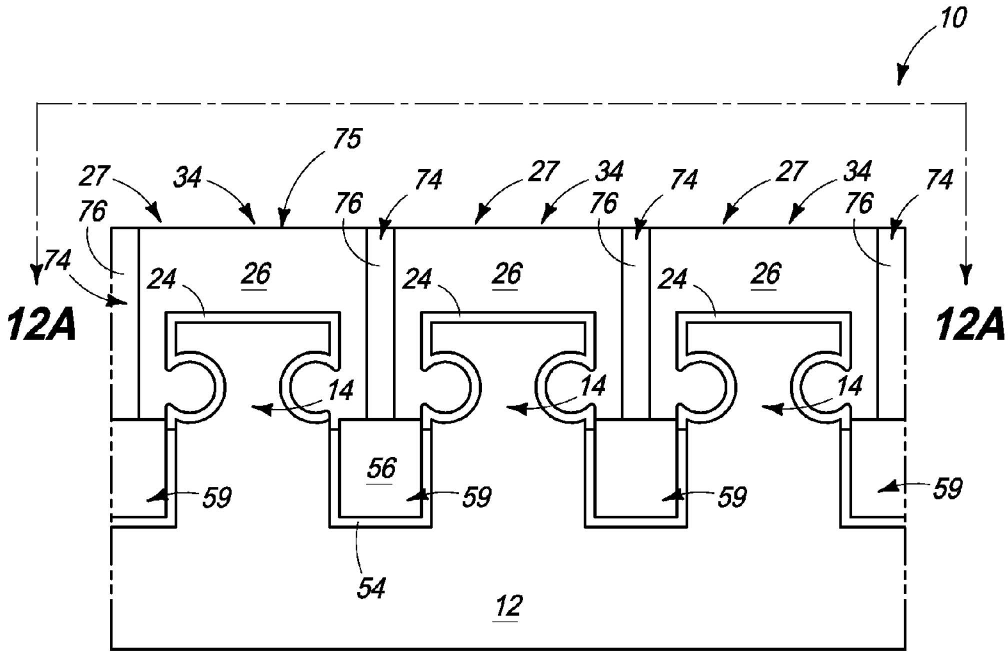


FIG. 12

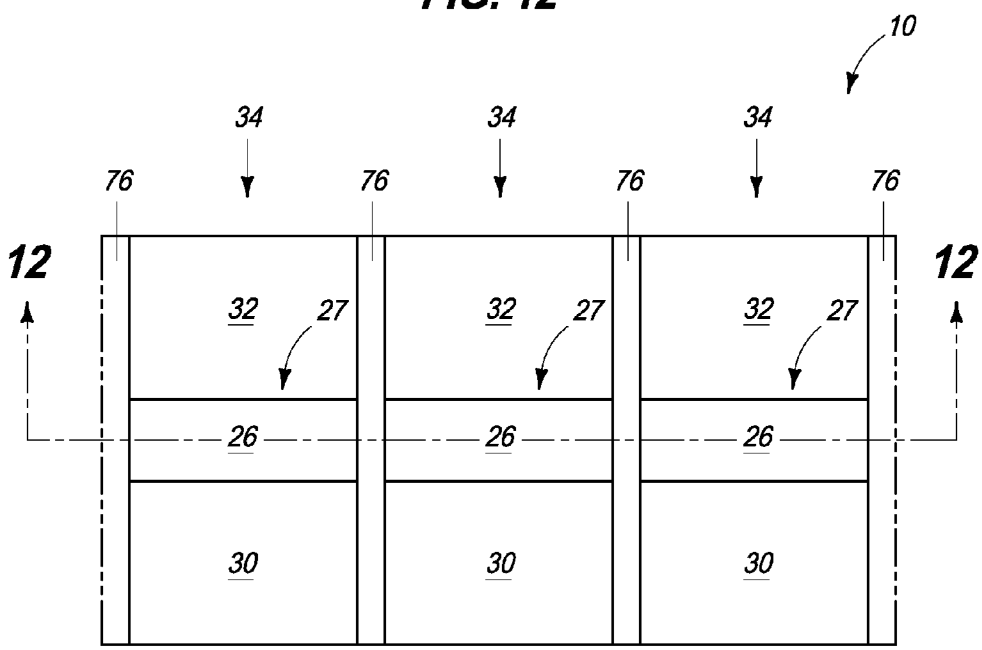


FIG. 12A

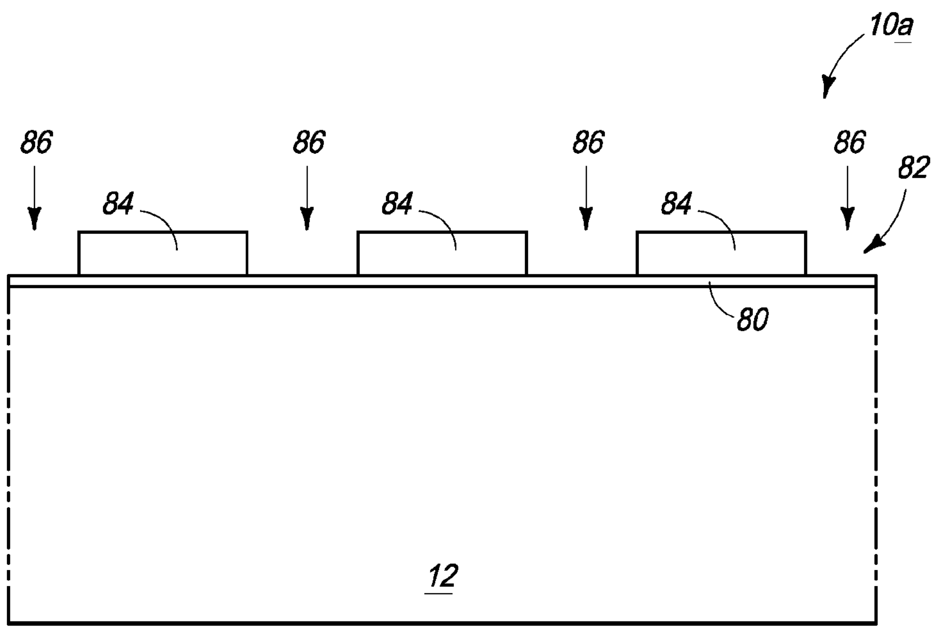
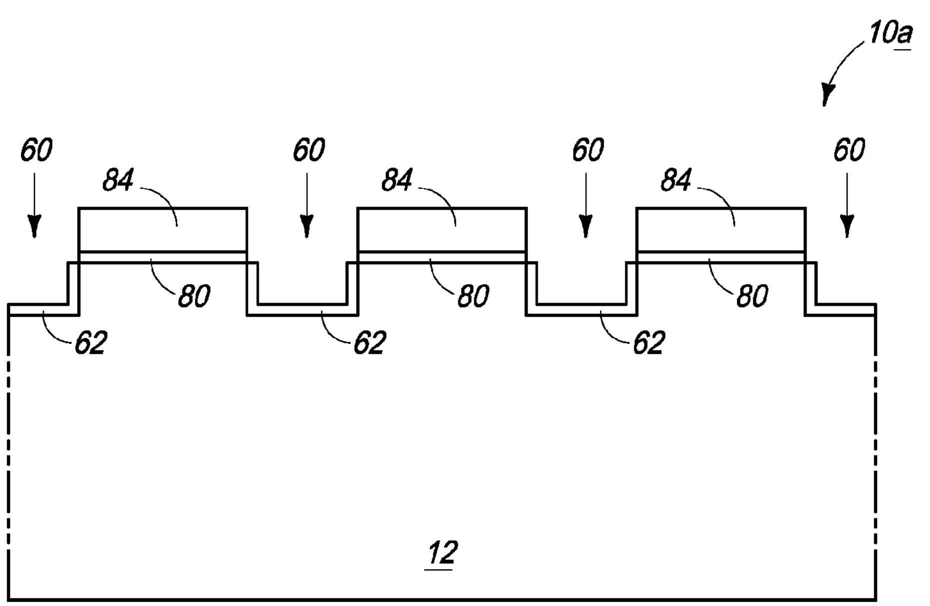

10a
86
86
86
86
82
84
84
84
80
12

FIG. 13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60
60
60
60
84
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80
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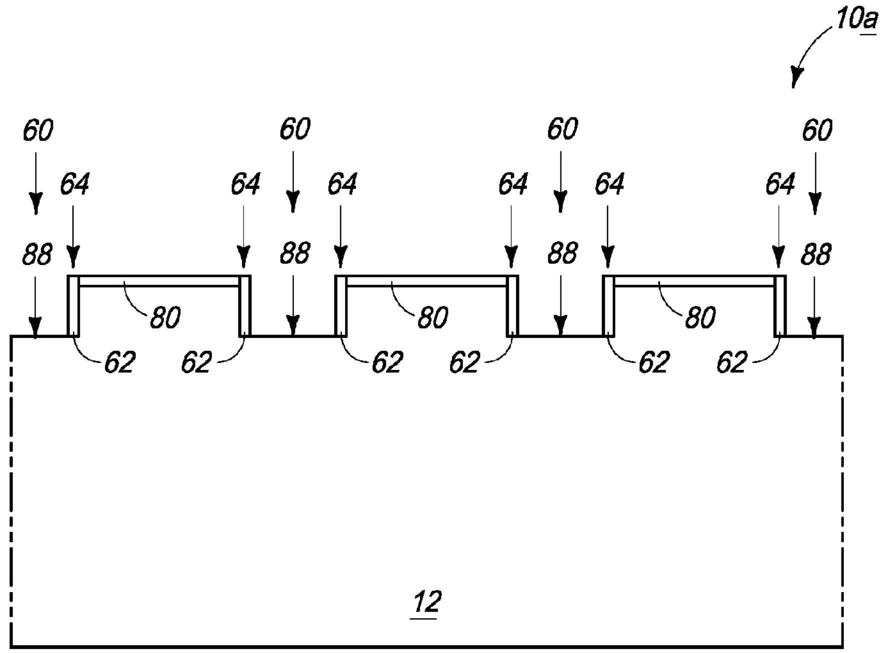
80
62
62
62
12

FIG. 14


10a
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64
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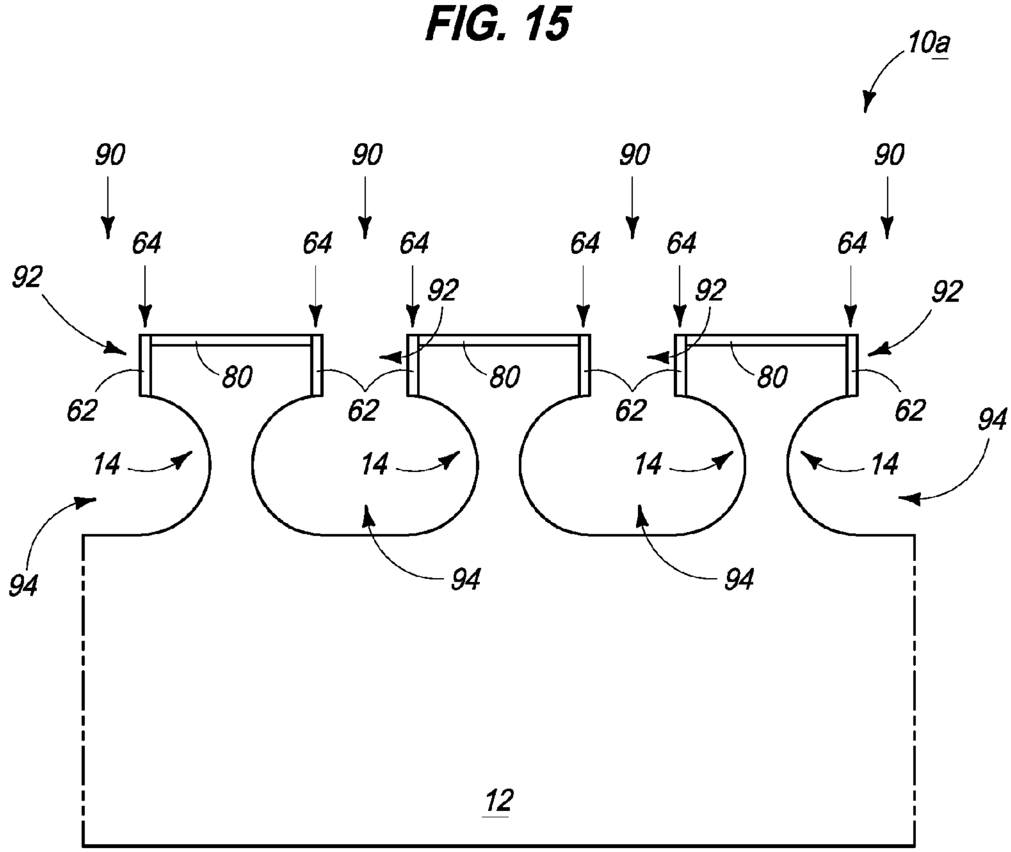
12

FIG. 15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64
64
92
92
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62
62
62
62
14
14
14
14
94
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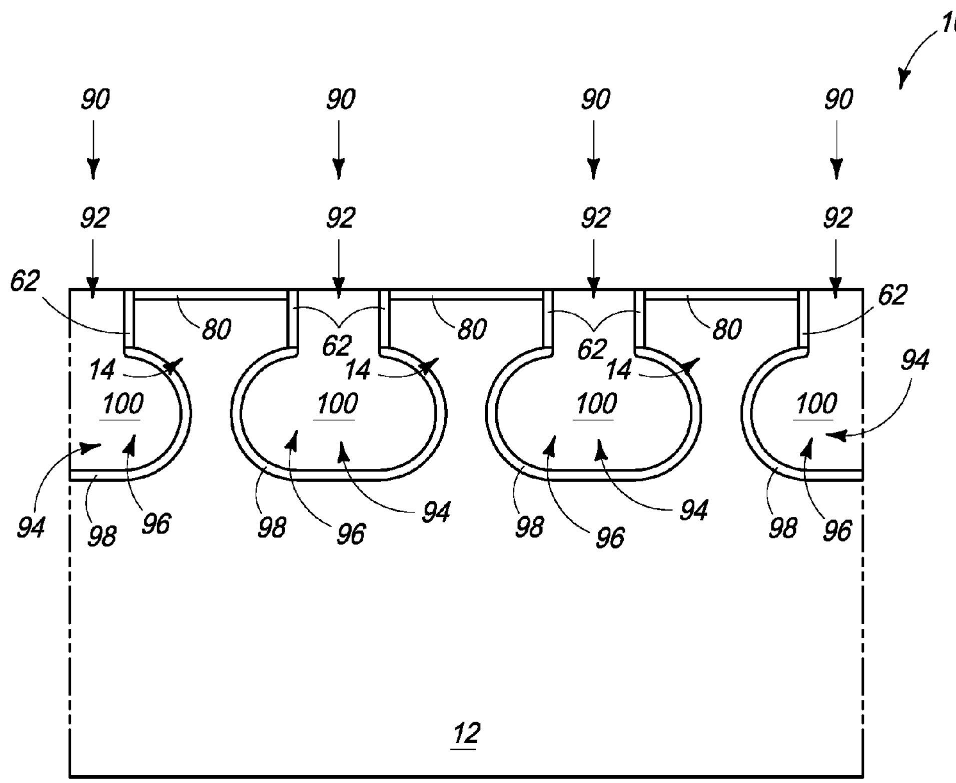
94
94
12

FIG. 16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62
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14
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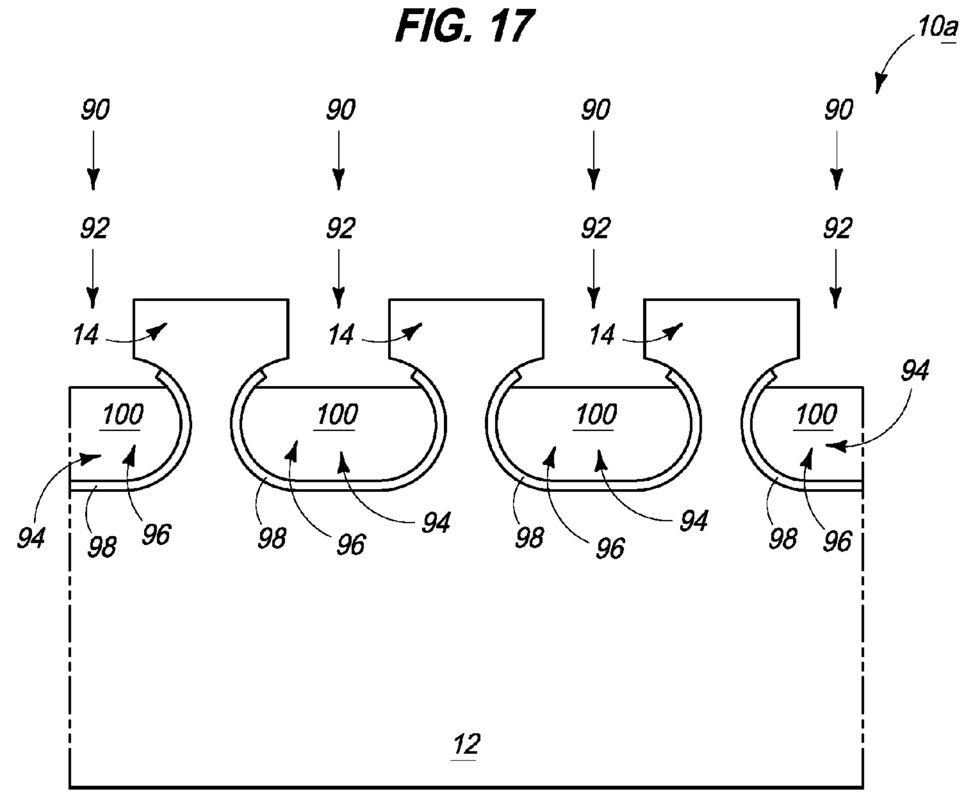
12

FIG. 17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14
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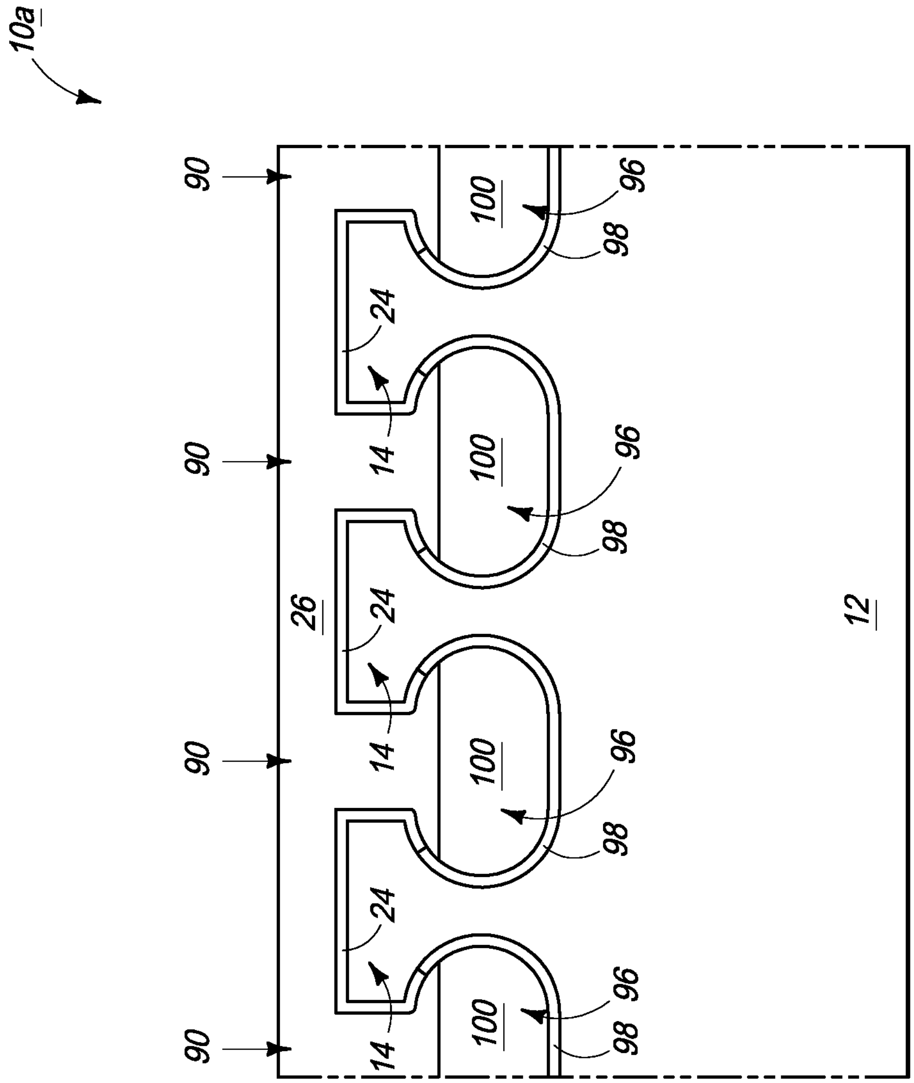
96
12

FIG. 18


10a
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90
100
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98
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24
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24
14
14
14
26
12

FIG. 19

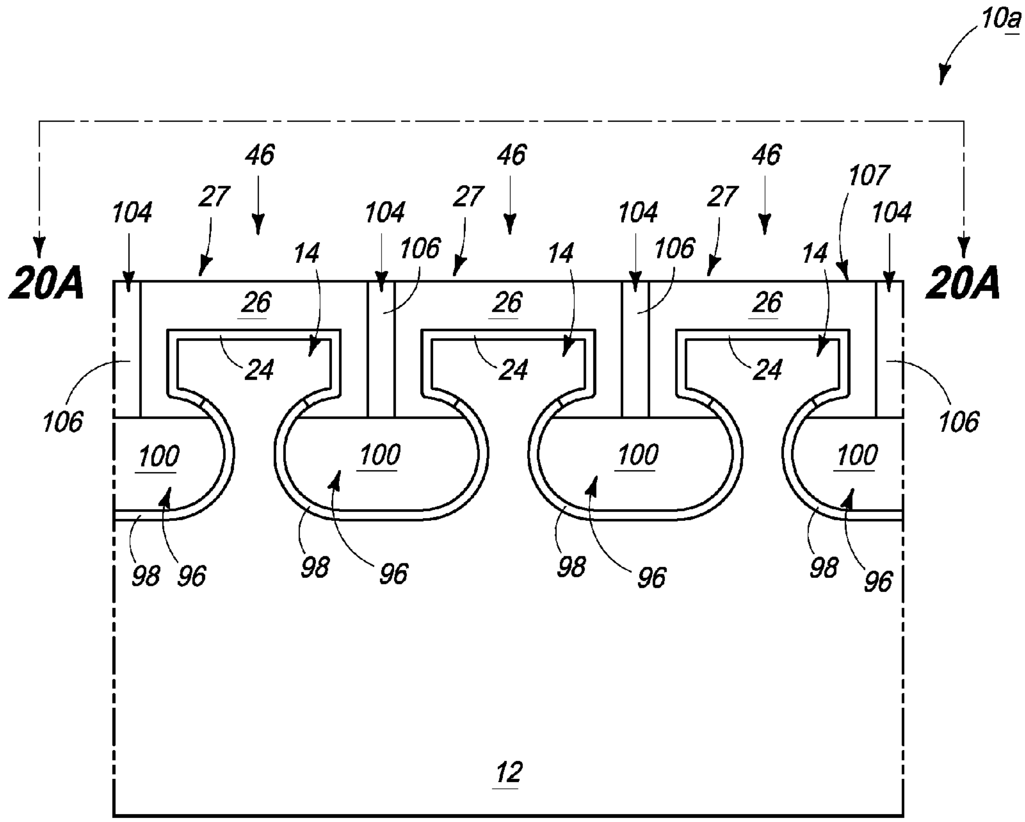

FIG. 20

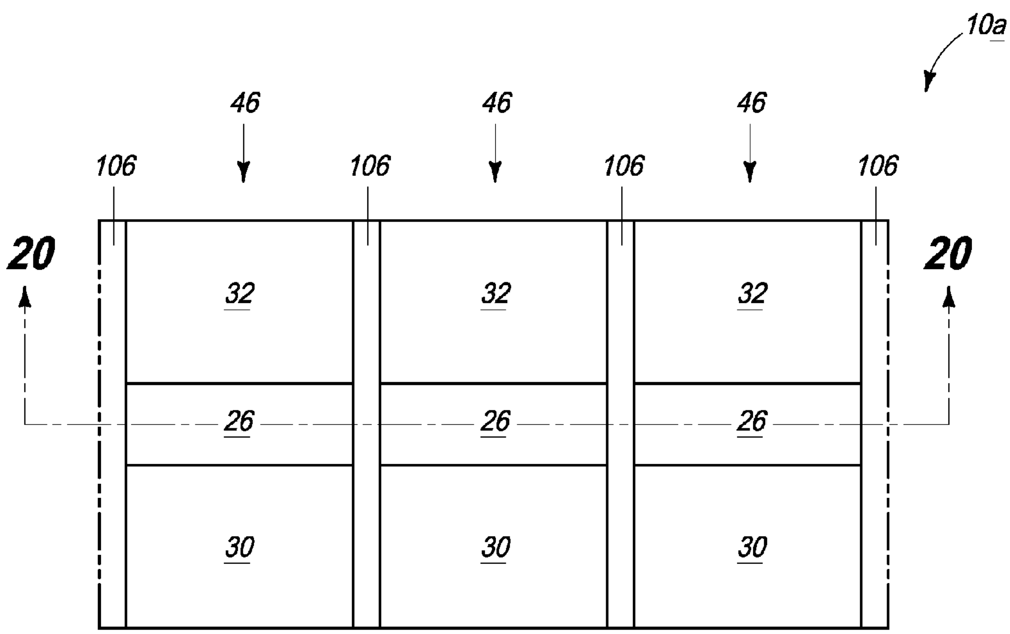

FIG. 20A

METHODS OF FORMING TRANSISTORS

TECHNICAL FIELD

Methods of forming transistors.

BACKGROUND

Transistors are commonly utilized in integrated circuits, and may have many applications throughout memory, logic, etc. For instance, transistors may be utilized in dynamic random access memory (DRAM) arrays, NAND flash, etc.

A continuing goal of integrated circuit fabrication is to create higher levels of integration, and accordingly to reduce size and spacing of existing components. It is becoming increasingly difficult to reduce the size of transistors due to short channel effects and other complications.

Transistor performance may be characterized by numerous metrics, including, for example, current flow through the on state (I_{on}) of the transistor and current flow through the off state (I_{off}) of the transistor. It is desired to have high I_{on} without leakage so that current is controlled and relatively unimpeded when the transistor is in the on state; and it is desired to have low I_{off}. Often there may be some level of leakage through transistors, especially as the transistors become increasingly smaller. An example leakage mechanism is hot electron induced punchthrough (HEIP), which can be particularly problematic in transistors having short channels.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** and **1**A are a cross-sectional side view and a top view, respectively, of a construction comprising an example embodiment transistor. The view of FIG. **1** is along the line **1-1** of FIG. **1**A, and the view of FIG. **1**A is along the line **1**A-**1**A of FIG. **1**.

FIGS. **2** and **2**A are a cross-sectional side view and a top view, respectively, of a construction comprising another example embodiment transistor. The view of FIG. **2** is along the line **2-2** of FIG. **2**A, and the view of FIG. **2**A is along the line **2**A-**2**A of FIG. **2**.

FIG. **3** is a cross-sectional side view of a construction comprising a plurality of transistors of the type shown in FIGS. **1** and **1**A.

FIG. **4** is a cross-sectional side view of a construction comprising a plurality of transistors of the type shown in FIGS. **2** and **2**A.

FIGS. **5-12** are diagrammatic cross-sectional views of various process stages of an example embodiment method of forming a plurality of transistors. FIG. **12**A is a top view of the construction of FIG. **12**. The view of FIG. **12** is along the line **12-12** of FIG. **12**A, and the view of FIG. **12**A is along the line **12**A-**12**A of FIG. **12**.

FIGS. **13-20** are diagrammatic cross-sectional views of various process stages of another example embodiment method of forming a plurality of transistors. FIG. **20**A is a top view of the construction of FIG. **20**. The view of FIG. **20** is along the line **20-20** of FIG. **20**A, and the view of FIG. **20**A is along the line **20**A-**20**A of FIG. **20**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Some embodiments include new methods of forming transistors. Example transistors that may be formed with such methods are described with reference to FIGS. **1** and **2**.

Referring to FIGS. **1** and **1**A, a construction **10** is shown in cross-sectional side view (FIG. **1**) and top view (FIG. **1**A). The construction includes a pillar **14** of semiconductor material **12**.

Semiconductor material **12** may comprise any suitable composition including, for example, silicon, germanium, silicon/carbon, silicon/germanium, etc. In some embodiments, the semiconductor material **12** may comprise, consist essentially of, or consist of monocrystalline silicon. The semiconductor material **12** may be considered to be part of a semiconductor substrate. The term "semiconductor substrate" means any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrates described above. In some embodiments, material **12** may be part of a semiconductor substrate containing one or more materials associated with integrated circuit fabrication. Some of the materials may be under the shown region of material **12** and/or may be laterally adjacent the shown region of material **12**; and may correspond to, for example, one or more of refractory metal materials, barrier materials, diffusion materials, insulator materials, etc.

Electrically insulative material **16** is along sidewalls of pillar **14**. The electrically insulative material may comprise any suitable composition or combination of compositions. In some embodiments, material **16** may comprise one or both of silicon dioxide and silicon nitride. For instance, material **16** may comprise primarily silicon nitride, but may additionally comprise a thin layer of silicon dioxide between the silicon nitride and surfaces of semiconductor material **12**.

The pillar **14** comprises a first wide region **18**, a narrow region **20**, and a second wide region **22**. In some embodiments, narrow region **20** may be referred to as a waist region. Gate dielectric material **24** extends along an upper portion of the pillar **14**; and specifically extends along an upper part of the first wide region **18** and along an entirety of the narrow region **20** and second wide region **22**.

The gate dielectric material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise, consist essentially of, or consist of silicon dioxide.

Electrically conductive gate material **26** extends along the upper portion of pillar **14**, and is spaced from the semiconductor material **12** by gate dielectric material **24**. The electrically conductive gate material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise, consist essentially of, or consist of one or more of various metals (for example, tungsten, titanium, etc.), metal-containing compositions (for instance, metal nitride, metal carbide, metal silicide, etc.), and conductively-doped semiconductor materials (for instance, conductively-doped silicon, conductively-doped germanium, etc.).

The gate material **26** and gate dielectric material **24** surround a channel region **28** of a transistor **34**. The top view of FIG. **1**A shows source/drain regions **30** and **32** formed within semiconductor material on opposing sides of a gate **27** comprising gate material **26**. In operation, source/drain regions **30** and **32** are gatedly connected to one another through gate **27**; and specifically are gatedly connected through electrical flow along channel region **28**.

The gate **27** may extend to any suitable depth relative to pillar **14**, and in some embodiments a bottom of the gate may be less than or equal to about 0.4 microns deep. Junction regions are present where the source/drain regions **30** and **32** interface with semiconductor material **12** (such junction regions are not visible in the views of FIGS. **1** and **1**A). In some embodiments, the junction regions may be within about 0.2 micron of the bottom of gate **27** (i.e., the depths of the junction regions may be within a range of from the depth of the bottom of the gate plus about 0.2 microns to the depth of the bottom of the gate minus about 0.2 microns).

Transistor **34** may be utilized in any of numerous applications; and may, for example, be incorporated into logic circuitry and/or memory circuitry. In some example applications, transistor **34** may be utilized in DRAM circuitry by connecting one of the source/drain regions **30** and **32** to a charge-storage device (for instance, a capacitor) and the other to a bitline. Accordingly, the transistor **34** may be incorporated into a DRAM unit cell. Such unit cell may be one of a large plurality of substantially identical unit cells utilized in a DRAM array.

Another example transistor construction is described with reference to a construction **10***a* in FIGS. **2** and **2**A. Similar numbering will be utilized in describing FIGS. **2** and **2**A as is used above in describing FIGS. **1** and **1**A where appropriate.

Construction **10***a* includes a pillar **14** of semiconductor material **12**, and comprises electrically insulative material **16** along sidewalls of pillar **14**.

The pillar **14** of FIGS. **2** and **2**A comprises a narrow stem **40** joining to a wide cap **42**. In some embodiments, narrow stem **40** may be referred to as a waist region, and cap **42** may be referred to as a wide region. Gate dielectric material **24** extends along an upper portion of the pillar **14**; and specifically extends along a portion of the narrow stem **40** and along an entirety of the wide cap **42**.

Electrically conductive gate material **26** extends along the upper portion of pillar **14**, and is spaced from the semiconductor material **12** by gate dielectric material **24**.

The gate material **26** and gate dielectric material **24** surround a channel region **44** of a transistor **46**. The transistor includes source/drain regions **30** and **32** formed within semiconductor material on opposing sides of a gate **27** comprising gate material **26**.

The transistors **34** and **46** of FIGS. **1** and **2** may advantageously consume less die area than conventional transistors for given performance due to increasing effective width, while also providing immunity towards hot electron induced punchthrough (HEIP) degradation and other punchthrough leakage mechanisms, thereby providing improved performance and reliability as compared to conventional transistors.

The transistors **34** and **46** of FIGS. **1** and **2** may be incorporated into memory arrays. FIGS. **3** and **4** illustrate regions of constructions **10** and **10***a*, respectively; comprising pluralities of transistors such as may be utilized in memory arrays.

Some embodiments pertain to methods of forming transistors of the types illustrated in FIGS. **1** and **2**. Example methods are described with reference to FIGS. **5**-**20**; with FIGS. **5**-**12** pertaining to an example method of forming transistors of the type described in FIGS. **1** and **3**, and with FIGS. **13**-**20** pertaining to an example method of forming transistors of the type described in FIGS. **2** and **4**.

Referring to FIG. **5**, construction **10** comprises semiconductor material **12**, and comprises a plurality of electrically insulative regions **50**-**53** extending into material **12**. The insulative regions **50**-**53** may be formed by initially forming cavities **49** extending into material **12**, and then filling the cavities with one or more insulative compositions. For instance, in the shown embodiment the cavities are lined with a first insulative composition **54**, and then filled with a second insulative composition **56**. In some embodiments, the first insulative composition may comprise silicon dioxide, and the second insulative composition may comprise silicon nitride. The material within cavities **49** may be referred to as first insulative material **59**; and accordingly in the shown embodiment such first insulative material comprises the two different compositions **54** and **56**. In other embodiments the first insulative material may comprise a single homogeneous composition, and in yet other embodiments the first insulative material may comprise more than two separate compositions.

A planarized surface **57** extends across the first insulative **59** and semiconductor material **12**. Such surface may be formed utilizing any suitable processing, including, for example, chemical-mechanical polishing (CMP).

A protective material **58** is formed across the planarized upper surface **57**. The protective material protects an upper surface of semiconductor material **12** during subsequent etching of a liner (described below), and during etching of first insulative material **59**. Material **58** may comprise any material suitable for providing such protection. Material **58** is a sacrificial material, and accordingly may comprise electrically conductive compositions and/or electrically insulative compositions. In some embodiments, material **58** may comprise one or more of metal, metal-containing compositions, metal-containing oxide, carbon, etc.

Referring to FIG. **6**, material **58** is patterned to form recesses **60** extending therethrough, and an upper portion of the first insulative material **59** is removed to extend such recesses into the cavities **49**. The material **58** may be patterned utilizing any suitable methodology, including, for example, utilization of a photolithographically-patterned photoresist mask (not shown), and/or a sublithographic mask (not shown).

Liner material **62** is formed within recesses **60**, and in the shown embodiment also extends across an upper surface of protective material **58**. The liner material is subsequently utilized to protect a region of semiconductor material **12** during etching of insulative material **59**, and during etching of another region of material **12**. The liner material may comprise any composition suitable for such purpose. The liner material is a sacrificial material, and accordingly may comprise an insulative composition or a conductive composition. In some embodiments, material **62** may comprise one or more of metal, metal-containing compositions, metal-containing oxide, carbon, etc.

Referring to FIG. **7**, material **62** is subjected to an anisotropic etch which patterns material **62** into liners **64** along sidewalls of recesses **60**.

Referring to FIG. **8**, an additional portion of first insulative **59** is removed to expose segments **66** of semiconductor material **12**. The exposed segments are vertically between the liner material **62** and the first insulative material **59**.

Referring to FIG. **9**, semiconductor material **12** is isotropically etched through the exposed segments **66** (FIG. **8**). The isotropic etching transforms recesses **60** (FIG. **8**) into openings **68** having narrow upper regions **70** and wide, bulbous lower regions **72**. The illustrated shape of regions **72** is one of many bulbous shapes that may be formed. Etching conditions may be altered to achieve desired shapes. In some example embodiments, the regions **72** may have sharper corners adjacent materials **62** and **54** than is shown, and/or the regions **72** may have larger radii than is shown.

Referring to FIG. **10**, liner material **62** (FIG. **9**) is removed, as is protective material **58** (FIG. **9**). The semiconductor material **12** of FIG. **10** has been patterned into a plurality of pillars **14** analogous to the pillar described above with reference to FIG. **1**.

Referring to FIG. **11**, gate dielectric material **24** is formed along sidewalls of openings **68**, and gate material **26** is formed within the openings and over the gate dielectric material. The gate material extends over regions of semiconductor material **12** between opening **68**.

Referring to FIG. **12**, openings **74** are formed to extend through the gate material **26** within openings **68** (FIG. **11**), and then the openings **74** are filled with second insulative material **76**. Such second insulative material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise one or both of silicon dioxide and silicon nitride. In some embodiments, second insulative material **76** may comprise a composition in common with first insulative material **59**; and in other embodiments second insulative material **76** may comprise entirely different compositions relative to the first insulative material **59**.

The second insulative material splits gate material **26** within each opening **68** (such gate material is shown in FIG. **11**) into two portions which are electrically isolated from one another, and which correspond to transistor gates **27**. Each of the transistor gates extends from one opening **68** to another (with the openings **68** being shown in FIG. **11**), and wraps around a pillar of semiconductor material between the openings.

A planarized surface **75** extends across materials **26** and **76**. Such planarized surface may be formed with any suitable processing, and in some embodiments may be formed utilizing CMP.

The construction of FIG. **12** comprises a plurality of transistors **34** analogous to the transistor described above with reference to FIG. **1**. A top view of FIG. **12** is shown in FIG. **12**A to illustrate that source/drain regions **30** and **32** may be formed on opposing sides of gates **27**.

Another example processing sequence of forming transistors is described with reference to FIGS. **13**-**20**.

FIG. **13** shows a construction **10***a* comprising semiconductor material **12**, comprising a protective material **80** over material **12**, and comprising a patterned mask **82** over material **80**. The mask **82** comprises masking material **84**. The patterned masking material **84** may comprise any suitable composition or combination of compositions; including, for example, photolithographically patterned photoresist and/or sub-lithographically patterned material (such as material patterned utilizing pitch-multiplication methodologies).

Protective material **80** may comprise any suitable composition or combination of compositions; and in some embodiments may comprise silicon nitride and/or silicon dioxide.

Gaps **86** extend through patterned mask **82**.

Referring to FIG. **14**, gaps **86** (FIG. **13**) are extended into semiconductor material **12** to form recesses **60**, and liner material **62** is formed within the recesses. The liner material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise silicon nitride and/or silicon dioxide.

Referring to FIG. **15**, material **62** is subjected to an anisotropic etch which patterns material **62** into liners **64** along sidewalls of recesses **60**. After material **62** is etched, segments **88** of semiconductor material **12** are exposed along bottoms of recesses **60**.

In the shown embodiment, masking material **84** (FIG. **14**) is removed prior to, or during, the anisotropic etching of liner material **62**.

Referring to FIG. **16**, semiconductor material **12** is isotropically etched through the exposed segments **88** (FIG. **15**). The isotropic etching transforms recesses **60** (FIG. **15**) into openings **90** having narrow upper regions **92** and wide, bulbous lower regions **94**. The illustrated shape of regions **94** is one of many bulbous shapes that may be formed. Etching conditions may be altered to achieve desired shapes. The semiconductor material **12** of FIG. **16** is patterned into a plurality of pillars **14** analogous to the pillar described above with reference to FIG. **2**.

Referring to FIG. **17**, insulative compositions **98** and **100** are formed within openings **90**. The compositions **98** and **100** may comprise silicon dioxide and silicon nitride, respectively, in some embodiments. The liner material **62** and protective material **80** are shown remaining along semiconductor material **12** at the processing stage of FIG. **17**. In other embodiments, one or both of materials **62** and **80** may be removed prior to forming compositions **98** and **100**; and in such embodiments material **98** may extend along the narrow upper regions **92** of openings **90**, and/or across upper surfaces of pillars **14**. The compositions **98** and **100** may be together referred to as a first insulative material **96** in some embodiments.

Referring to FIG. **18**, liner material **62** (FIG. **17**) and protective material **80** (FIG. **17**) are removed. The first insulative material **96** is recessed within openings **90** until the wide lower regions **94** of the openings are only partially filled with insulative material **96**. In some embodiments, the wide regions may be more than half-filled with insulative material **96** at the processing stage of FIG. **18**, and in other embodiments there may be less than half-filled.

In the shown embodiment of FIG. **18**, composition **100** is recessed further than composition **98**. In other embodiments, compositions **98** and **100** may be recessed to about a same extent as one another, and in yet other embodiments composition **98** may be recessed further than composition **100**.

Referring to FIG. **19**, gate dielectric material **24** is formed along sidewalls of openings **90**, and gate material **26** is formed within the openings and over the gate dielectric material. The gate material **26** and gate dielectric material **24** extend over regions of semiconductor material **12** between openings **90**.

Referring to FIG. **20**, openings **104** are formed to extend through the gate material **26** within openings **90** (FIG. **19**), and then the openings **104** are filled with second insulative material **106**. Such second insulative material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise one or both of silicon dioxide and silicon nitride. In some embodiments, second insulative material **106** may comprise a composition in common with first insulative material **96**, and in other embodiments second insulative material **106** may comprise entirely different compositions relative to the first insulative material **96**.

The second insulative material **106** splits gate material **26** within each opening **90** (such gate material is shown in FIG. **19**) into two portions which are electrically isolated from one another, and which correspond to transistor gates **27**. Each of the transistor gates extends from one opening **90** to another (with the openings **90** being shown in FIG. **19**), and wraps around a pillar of semiconductor material between the openings.

A planarized surface **107** extends across materials **26** and **106**. Such planarized surface may be formed with any suitable processing, and in some embodiments may be formed utilizing CMP.

The construction of FIG. **20** comprises a plurality of transistors **46** analogous to the transistor described above with reference to FIG. **2**. A top view of FIG. **20** is shown in FIG. **20**A to illustrate that source/drain regions **30** and **32** may be formed on opposing sides of gates **27**.

The structures and devices discussed above may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

Unless specified otherwise, the various materials, substances, compositions, etc. described herein may be formed with any suitable methodologies, either now known or yet to be developed, including, for example, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.

The terms "dielectric" and "electrically insulative" are both utilized to describe materials having insulative electrical properties. Both terms are considered synonymous in this disclosure. The utilization of the term "dielectric" in some instances, and the term "electrically insulative" in other instances, is to provide language variation within this disclosure to simplify antecedent basis within the claims that follow, and is not utilized to indicate any significant chemical or electrical differences.

The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regardless of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

The cross-sectional views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings.

When a structure is referred to above as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

Some embodiments include a method of forming a transistor. Spaced-apart recesses are formed to extend into semiconductor material. The recesses have upper regions lined with liner material and have segments of semiconductor material exposed along lower regions. Semiconductor material is isotropically etched through the exposed segments while the upper regions remain protected with the liner material. The isotropic etching transforms the recesses into openings having wide lower regions beneath narrow upper regions. The liner material is removed. Gate dielectric material is formed along sidewalls of the openings. Gate material is formed within the openings and over regions of the semiconductor material between the openings. Insulative material is formed down the center of each opening and entirely through the gate material. The insulative material splits the gate material within each opening into two isolated portions. A segment of gate material extends from one of the openings to the other, and wraps around a pillar of the semiconductor material between the openings. The segment is a gate of a transistor. Source/drain regions are formed on opposing sides of the gate.

Some embodiments include a method of forming a transistor. Spaced-apart recesses are formed to extend into semiconductor material. Sidewalls of the recesses are lined with liner material while leaving bottoms of the recesses exposed. Semiconductor material is isotropically etched through the exposed bottoms of the recesses while the sidewalls remain protected with the liner material. The isotropic etching transforms the recesses into openings having bulbous lower regions beneath narrow upper regions. The liner material is removed. Gate dielectric material is formed along sidewalls of the openings. Gate material is formed within the openings and over regions of the semiconductor material between the openings. Insulative material is formed down the center of each opening and entirely through the gate material. The insulative material splits the gate material within each opening into two isolated portions. A segment of gate material extends from one of the openings to the other, and wraps around a pillar of the semiconductor material between the openings. The segment is a gate of a transistor. Source/drain regions are formed on opposing sides of the gate.

Some embodiments include a method of forming a transistor. Spaced-apart cavities are formed to extend into semiconductor material, and the cavities are filled with first insulative material. Some the first insulative material is removed from the cavities to leave recesses extending into the cavities. Liner material is formed along sidewalls of the recesses. After the liner material is formed, some of the first insulative material is removed to leave exposed segments of semiconductor material between the liner material and the first insulative material. Semiconductor material is isotropically etched through the exposed segments while the sidewalls remain protected with the liner material. The isotropic etching transforms the recesses into openings having bulbous lower regions beneath narrow upper regions. The liner material is removed. Gate dielectric material is formed along sidewalls of the openings. Gate material is formed within the openings and over regions of the semiconductor material between the openings. Second insulative material is formed down the center of each opening and entirely through the gate material. The second insulative material splits the gate material within each opening into two isolated portions. A segment of gate material extends from one of the openings to the other, and wraps around a pillar of the semiconductor material between the openings. The segment is a gate of a transistor. Source/drain regions are formed on opposing sides of the gate.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

We claim:

1. A method of forming a transistor, comprising:

forming a pair of spaced-apart recesses extending into semiconductor material, the recesses having upper regions lined with liner material and having segments of semiconductor material exposed along lower regions;

isotropically etching semiconductor material through the exposed segments while the upper regions remain protected with the liner material; the isotropic etching transforming the recesses into openings having wide lower regions beneath narrow upper regions;

removing the liner material;

forming gate dielectric material along sidewalls of the openings;

forming gate material within the openings and over regions of the semiconductor material between the openings;

forming insulative material down the center of each opening and entirely through the gate material; the insulative material splitting the gate material within each opening into two isolated portions; a segment of gate material extending from one of the openings to the other, and wrapping around a pillar of the semiconductor material between the openings; said segment being a gate of a transistor; and

forming source/drain regions on opposing sides of the gate.

2. The method of claim **1** wherein the gate material extends to a depth of less than or equal to about 0.4 microns within the semiconductor material.

3. The method of claim **1** wherein the wide regions are bulbous regions.

4. The method of claim **1** wherein the pillar has a shape of a narrow waist region extending upwardly to a wide region, and wherein the gate material is along a region of the narrow waist and under the wide region.

5. The method of claim **1** wherein the pillar has a shape of a first wide region, narrow region over the first wide region, and second wide region over the narrow region; and wherein the gate material is along the narrow region and second wide region, and along a portion of the first wide region.

6. The method of claim **1** wherein the insulative material comprises silicon nitride.

7. The method of claim **1** wherein bottoms of the recesses are along semiconductor material.

8. The method of claim **1** wherein the insulative material is second insulative material, and further comprising forming first insulative material within the openings prior to forming the gate material.

9. The method of claim **8** wherein the first insulative material is formed to fill the openings, and is recessed to only partially fill the openings prior to forming the gate material.

10. The method of claim **9** wherein the first and second insulative materials comprise a common composition as one another.

11. The method of claim **10** wherein the first and second insulative materials both comprise silicon nitride.

12. The method of claim **9** wherein the first and second insulative materials do not comprise a common composition as one another.

13. The method of claim **1** wherein the insulative material is second insulative material, and wherein bottoms of the recesses are along first insulative material.

14. The method of claim **13** wherein the first insulative material comprises silicon nitride.

15. The method of claim **13** wherein the first insulative material comprises silicon dioxide and silicon nitride.

16. A method of forming a transistor, comprising:

forming a pair of spaced-apart recesses extending into semiconductor material;

lining sidewalls of the recesses with liner material while leaving bottoms of the recesses exposed;

isotropically etching semiconductor material through the exposed bottoms of the recesses while the sidewalls remain protected with the liner material; the isotropic etching transforming the recesses into openings having bulbous lower regions beneath narrow upper regions;

removing the liner material;

forming gate dielectric material along sidewalls of the openings;

forming gate material within the openings and over regions of the semiconductor material between the openings;

forming insulative material down the center of each opening and entirely through the gate material; the insulative material splitting the gate material within each opening into two isolated portions; a segment of gate material extending from one of the openings to the other, and wrapping around a pillar of the semiconductor material between the openings; said segment being a gate of a transistor; and

forming source/drain regions on opposing sides of the gate.

17. The method of claim **16** wherein the pillar has a shape of a narrow stem extending upwardly to a wide cap, and wherein the gate material is along a region of the narrow stem and under the wide cap.

18. The method of claim **16** wherein the insulative material is a second insulative material, and further comprising:

filling the openings with first insulative material;

recessing the first insulative material until the bulbous lower regions are only partially filled with the first insulative material; and

forming the gate material within the partially-filled openings.

19. The method of claim **18** wherein the partially-filled openings have bulbous regions more than half-filled with the first insulative material.

20. The method of claim **18** wherein the partially-filled openings have bulbous regions less than half-filled with the first insulative material.

21. The method of claim **18** wherein the first and second insulative materials comprise a same composition as one another.

22. The method of claim **18** wherein the first and second insulative materials both comprise silicon nitride.

23. The method of claim **18** wherein the first and second insulative materials comprise different compositions relative to one another.

24. A method of forming a transistor, comprising:

forming a pair of spaced-apart cavities extending into semiconductor material, and filling the cavities with first insulative material;

removing some the first insulative material from the cavities to leave recesses extending into the cavities, and forming liner material along sidewalls of the recesses;

after forming the liner material, removing some of the first insulative material to leave exposed segments of semiconductor material between the liner material and the first insulative material;

isotropically etching semiconductor material through the exposed segments while the sidewalls remain protected with the liner material; the isotropic etching transforming the recesses into openings having bulbous lower regions beneath narrow upper regions;

removing the liner material;

forming gate dielectric material along sidewalls of the openings;

forming gate material within the openings and over regions of the semiconductor material between the openings;

forming second insulative material down the center of each opening and entirely through the gate material; the second insulative material splitting the gate material within each opening into two isolated portions; a segment of gate material extending from one of the openings to the other, and wrapping around a pillar of the semiconductor material between the openings; said segment being a gate of a transistor; and

forming source/drain regions on opposing sides of the gate.

25. The method of claim **24** wherein the pillar has a shape of a narrow waist region extending upwardly to a wide region, and wherein the gate material is along the narrow waist region and under the wide region.

26. The method of claim **24** wherein the pillar has a shape of a first wide region, narrow region over the first wide region, and second wide region over the narrow region; and wherein the gate material is along the narrow region and second wide region, and along a portion of the first wide region.

27. The method of claim **24** wherein the first insulative material comprises silicon nitride.

28. The method of claim **24** wherein the first insulative material comprises silicon dioxide.

29. The method of claim **24** wherein the first insulative material comprises silicon dioxide and silicon nitride.

30. The method of claim **24** wherein the second insulative material comprises silicon nitride.

31. The method of claim **24** wherein the first and second insulative materials comprises a same composition as one another.

32. The method of claim **24** wherein the first and second insulative materials comprises different compositions relative to one another.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 9,147,729 B2
APPLICATION NO. : 14/189296
DATED : September 29, 2015
INVENTOR(S) : Deepak Chandra Pandey et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Column 10, line 46: insert --of-- after --some--.

Signed and Sealed this
Twenty-first Day of June, 2016

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office